AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Original) A coding cell of a nonvolatile ferroelectric memory device, comprising:

a first latch having one node connected with a first node and the other node connected with second and third nodes;

a first transistor having a gate terminal to which a gate control signal is input, a source terminal to which a signal of the second node is transferred, and a drain terminal to which a first data signal is input;

a second transistor having a gate terminal to which the gate control signal is input, a source terminal to which a signal of the third node is transferred, and a drain terminal to which a second

data signal is input;

a second latch having one node connected with a fourth node and the other node connected with the second and third nodes;

a first ferroelectric capacitor arranged between an input terminal of a control signal and the second node;

a second ferroelectric capacitor arranged between the input terminal of the control signal and the third node;

a third ferroelectric capacitor arranged between the second node and a voltage terminal; and

a fourth ferroelectric capacitor arranged between the third node and the voltage terminal.

18. (Original) The coding cell of claim 17, further comprising an equalizing block between the second and third nodes.

19. (Original) The coding cell of claim 17, further comprising a switching block operating in response to signals of the second and third nodes.

20. (Original) A coding cell of nonvolatile of ferroelectric memory device, comprising:

a PMOS transistor transferring a power source voltage VCC to a first node in response to a first control signal;

a first latch having one node connected with the first node and

the other node connected with second and third nodes;

a first transistor having a gate terminal to which a gate control signal is input, a source terminal to which a signal of the second node is transferred, and a drain terminal to which a first data signal is input;

a second transistor having a gate terminal to which the gate control signal is input, a source terminal to which a signal of the third node is transferred, and a drain terminal to which a second data signal is input;

a third transistor transferring a ground voltage VSS to a fourth node in response to a second control signal;

a second latch having one node connected with the fourth node and the other node connected with the second and third nodes;

a switching block operating in response to signals of the second and third nodes;

a first ferroelectric capacitor arranged between an input terminal of a third control signal and the second node;

a second ferroelectric capacitor arranged between the input terminal of the third control signal and the third node;

a third ferroelectric capacitor arranged between the second node and a voltage terminal; and

a fourth ferroelectric capacitor arranged between the third node and the voltage terminal.

21. (Original) The coding cell of claim 20, further comprising an equalizing block between the second and third nodes.

22. (Original) The coding cell of claim 20, further comprising a switching block operating in response to signals of the second and third nodes.

23. (Canceled)

24. (Canceled)